REMARKS

This responds to the Office Action mailed on January 24, 2008.

No claims are amended. Claims 25-49 are pending in this application.

§102 Rejection of the Claims

Claims 25-29, 31-33, 36-39, 41, 43-45, and 49 were rejected under 35 U.S.C. § 102(b) for anticipation by Morse et al. (U.S. Patent No. 6,351,326 B1). This rejection is respectfully traversed. Morse does not teach or suggest a PIN diode structure as claimed in each of the independent claims.

Claim 1 describes a optical resonant silicon cavity with a P-I-N diode formed about it, such that the resonant cavity forms an intrinsic, non-active region of the P-I-N diode. Morse et al., describes a capacitive structure, not a P-I-N diode. Not only is the structure different, but the ability of the presently claimed structure to inject carriers is simply not present in the Morse et al., device.

The Office Action indicates that Morse et al., at column 5, lines 26-44 describes p+ and n+ doped areas with the optical resonant cavity forms an intrinsic non-active region of a PIN diode. This is respectfully traversed, as the description corresponds to that of a capacitor, not a PIN diode. The language cited even refers to capacitor like charge accumulation in the polysilicon regions 117 and 118:

> "In the illustrated example, it is assumed that a higher voltage V1 is applied to polysilicon region 117 by signal 129 and a lower voltage V2 is applied to polysilicon region 118 by signal 131. In this embodiment, a net positive charge is then accumulated in polysilicon regions 117 and a net negative charge is accumulated in polysilicon regions 118. In an embodiment in which polysilicon regions 117 and 118 include p-type doped semiconductor material, a positive charge causes accumulation of holes near the borders with the regions of dielectric layer 105, while a negative charge causes depletion of holes near the borders with the regions of dielectric layer 105. In an embodiment in which polysilicon regions 117 and 118 include n-type doped semiconductor material, a positive charge causes depletion of electrons near the borders with the regions of dielectric layer

105, while a negative charge causes accumulation of electrons near the borders with the regions of dielectric layer 105."

The cited langauge also clearly indicates that the structure of Morse et al., operates by accumulation and depletion of carriers, not carrier injection. This is a direct result of the capacitive structure described by Morse et al., and further supports the fact that it is not a PIN structure. Since Morse et al., does not describe a PIN structure as claimed in each of the independent claims 15, 36, 48 and 49, it is requested that the rejection be withdrawn.

Dependent claim 26 positively recites what the structure of independent claim 25 provides, injection of carriers via the application of a voltage across the p+ and n+ areas of the PIN diode. Since Morse et al., does not teach or disclose a PIN diode, and also even the cited language by the Office Action describes carrier depletion and accumulation and not carrier injection, the rejection should be withdrawn.

Claim 33 depends from claim 25, and further recites that the optical resonant cavity is a planar micro cavity. Morse et al., describes a stack of periodically spaced polysilicon or silicon regions 117, 118 in a dielectric layer. This structure is clearly not a planar micro cavity. The Office Action refers to FIGs. 1 and 2, but does not identify any specific structure in such figures as corresponding to the planar micro cavity.

The claims depending from the independent claims are believed allowable for at least the same reasons as the independent claims.

§103 Rejection of the Claims

Claims 30, 34-35, 40, 42, and 46-48 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Morse et al. (U.S. Patent No. 6,351,326 B1) in view of Morse (U.S. Patent No. 6,876,050 B2). This rejection is respectfully traversed.

Claims 30, 34-35, 40, 42 and 46-48 are believed to distinguish from Morse et al., for at least the same reasons as independent claim 25, and should be allowable as such. Further, the Office Action indicates that Morse is illustrative of the fact that rib waveguides and trenches in silicon electro optic modulators are well known in the art and cites some of their advantages as well known. This assertion is respectfully traversed, as Morse, similarly to Morse et al., describes the use of capacitive structures, and no teaching is provided of the stated advantages in

conjunction with the use of a PIN diode as claimed. In addition neither Morse, nor the advantages cited would teach or suggest to one of ordinary skill in the art to create a structure with a PIN diode to modulate carrier concentration within an optical resonant cavity. Thus these claims are also believed patentable and it is requested that the rejection be withdrawn.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have equally addressed every assertion made in the Office Action, however, this does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6972 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 5-8-2008

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 8th day of May 2008.

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